PCI-SIG® DevCon 2015 Update

Al Yanes, President and Chairman

Ramin Neshati, Marketing Workgroup Chair

About PCI-SIG

Organization that **defines I/O bus specifications** and **related form factors**.

- 750+ member companies located around the world

Creating specifications and mechanisms to **support compliance** and **interoperability.**

- **Australia**
- **Brazil**
- **China**
- **Egypt**
- **France**
- **Germany**
- **Israel**
- **Italy**
- **Japan**
- **Korea**
- **Taiwan**
- **USA**

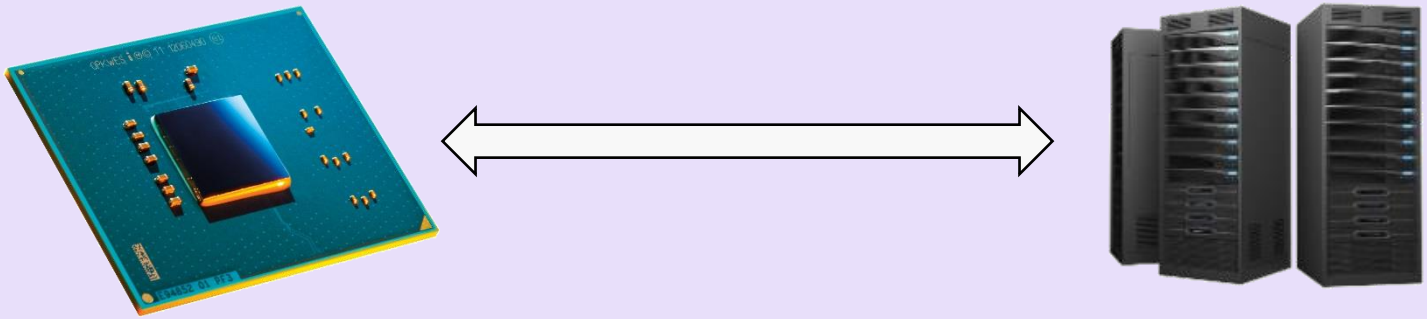
Board of Directors 2015-2016

AMD, DELL, hp, IBM, intel, lenovo, NVIDIA, QUALCOMM, SYNOPSYS® Silicon to Software™

Evolving I/O Market

PCI-SIG delivers a **low-cost**, **high-performance, ubiquitous and robust** interconnect for the computing industry.

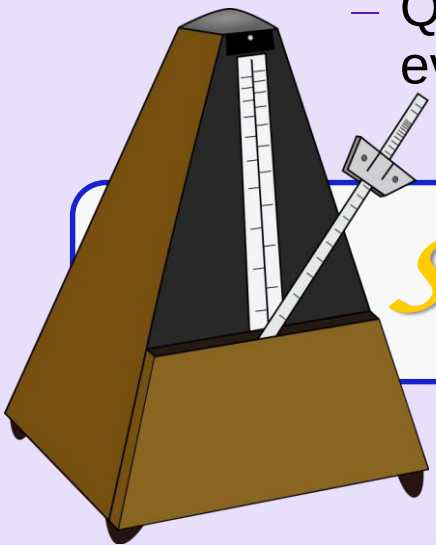
The explosive growth in the IoT and mobile device markets has led to increased demand for low power, high performance I/O.



PCIe Adoption Across the Industry

PCI-SIG's Low Power Initiatives

- Enhanced PCIe base specifications to reduce power consumption
  - ✓ L1 Sub-states
    - Improves energy distribution on platforms
    - Lowers idle power in sleep mode
  - ✓ Half-swing and quarter-swing specifications
    - Half-swing was introduced in PCIe 1.0 base spec
    - Quarter-swing takes power even lower in PCIe 4.0



Swing low

PCI-SIG's Low Power Initiatives

- Extended PCIe architecture to the mobile and handheld industry with the M-PCIe specification
  - ✓ PCIe architecture adapted to operate over the MIPI® Alliance low-power M-PHY® technology
- Expanded PCIe applications to low power and battery-based applications
  - ✓ Embedded, handheld, mobile devices etc.
- Flexible lane width configurations and speed selection supporting low power solutions
  - ✓ Desktops, servers and storage solutions

Our Focus

- Markets and Applications
  - ✓ PC, Servers, Mobile, SoC, Storage, IoT, Network, Accelerators, etc.
  - ✓ Architecture is well-suited for low-power implementations
    - Half-swing and quarter-swing
    - L1 Sub-states
    - M-PCIe™
- New Form Factors
  - ✓ M.2 for mobile platforms and new BGA form factor
  - ✓ SFF-8639 for high-density SSD storage attach
  - ✓ OCuLink for low-cost disaggregation
- Evolving Specification for Increased Performance
  - ✓ PCIe 4.0 technology @ 16GT/s

PCIe 4.0 for Big Data Applications

- **16GT/s bit rate with full compatibility**
  - ✓ Meets Big Data application requirements at lowest cost
    - HPC, Data Center, workstation/client platforms, embedded systems, peripheral devices, and more
    - HVM processes and materials
  - ✓ Doubles I/O bandwidth over PCIe 3.0 specification
    - Preserves backward compatibility with all previous PCIe specifications
  - ✓ Low-cost, high-performance I/O technology
    - Facilitates narrower link widths and cost savings through pin reduction
  - ✓ Rev 0.7 anticipated for Q4
  - ✓ Rev 0.9 targeted: 2H 2016

	Raw Bit Rate	Link BW	BW/Lane/Way	Total BW x16
PCIe 1.x	2.5GT/s	2Gb/s	~250MB/s	~8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	~500MB/s	~16GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s

PCIe Technology Portfolio

PCIe Ecosystem

Delivering a consistent and interoperable user experience across multiple platforms

High performance I/O with low power features

2002 to present…

High performance and low power for handheld devices

2013 to present…

- Industry-leading compliance program
- Native OS support for device discovery and configuration
- Many lines of code, delivering ubiquitous software solutions

Summary

PCI-SIG continues its legacy of delivering high-performance, low-power specifications for multiple applications and markets

- PCIe 4.0 base specification
  - ✓ Rev 0.7 expected in Q4
- OCuLink low cost, small cable form factor
  - ✓ Rev 0.9 under review; Rev 1.0 expected in Q3
- M.2 specification
  - ✓ New BGA form factor and electrical pin-out being defined
- SFF-8639 server module for high-density SSD storage attach
  - ✓ FYI testing at August workshop, Compliance Workshop #94

2015 PCI-SIG DevCon

SPONSOR COMPANIES

Sponsor Company Presenters

Platinum	cadence™	**Booth 8** – Arif Khan, Product Marketing Director
	KEYSIGHT TECHNOLOGIES	**Booth 7** – Rick Eads, Principal Product Manager
	SYNOPSYS® Silicon to Software™	**Booth 9** – Scott Knowlton, Sr. Product Marketing Manager
Silver	PLDA	**Booth 2** – Gary Ruggles, Sales Director
Exhibitor	Mellanox® TECHNOLOGIES	**Booth 13** – Scot Schultz, Director, HPC & Technical Computing
	NEC	**Booth 12** – Shinji Abe, Senior Manager, Product Architect
	SerialTek	**Booth 1** – Steve Wong, Director, Marketing & Product Mgmt
	Tektronix®	**Booth 11** – Sarah Boen, Product Marketing Manager

Cadence

- Visit our booth (#8) and see our exciting demos
  - ✓ 16FF PCIe PHY Gen 4 PHY for high-performance applications
    - *High performance PHY highlighting actual eye mask and available margins with built in diagnostics*
  - ✓ PCIe 4.0 Controller Solution
    - *View Cadence's PCIe 4.0 Controller solution that complements the PHY offering. Speak with our architect on how we can accelerate your design.*
  - ✓ PCIe 2.0/3.0 Controller and 16FF PHY for mobile applications
    - *Accelerating your time to market with silicon proven solutions in leading edge nodes*
  - ✓ Indago Protocol Debug App
    - *Verification challenges mount as ARM® AMBA®, DDR, USB, PCIe, MIPI and other protocol families continue to expand in variety and complexity. The Indago Protocol Debug App cuts debug effort by up to 50% by clearly correlating SoC behavior to the protocol specification.*

Booth #8

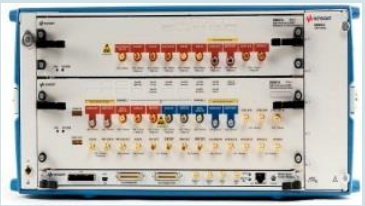
Keysight Technologies

Keysight's New PCI Express® Solutions

NEW!

Simulation

Physical layer receiver test



Data link / transaction layer

W2352EP

Compliance Test Bench for PCIe®

for Advanced Design System (ADS)

M8041A

Adjustable ISI and Interactive Link Training for PCIe®

on the M8020A J-BERT

U4305B Exerciser

with L1 substate analysis for validation of 2.5, 5 and 8 Gbps PCIe® and LTSSM operation

Booth #7

Synopsys

DesignWare IP for PCI Express

Reduces Risk; Used in >1200 Products Across All Market Segments

Market	Trends	Synopsys Solutions
Enterprise Servers Networking Storage	• PCIe 3.0 → PCIe 4.0 • Low-power servers • PCIe/NVMe SSDs • RAS	• PCIe 4.0 PHY/Controller • PCIe 4.0 Interop Synopsys/Mellanox • PCIe 4.0 Verification IP w/controller • PCIe 4.0 & RAS for Enterprise
Mobile Wireless Multimedia	• PCIe 2.0 → PCIe 3.0 • Low power w/L1 sub-states & power gating	Industry's Lowest Power PCIe 3.1 Solution for Mobile SoCs
Consumer Digital Office Digital Home	• PCIe 1.0 → PCIe 2.0 • All about cost • Wirebond	Industry's First PCI-SIG Compliant PCIe Root Port IP

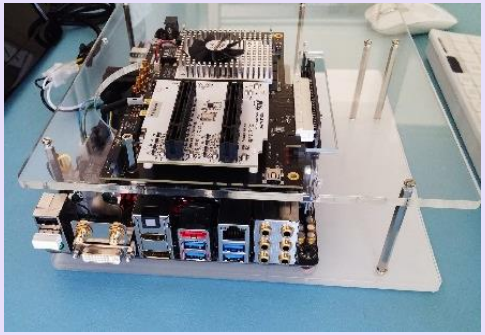
Booth #9

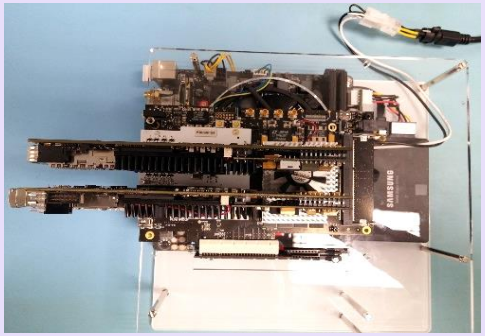
PLDA

Visit the PLDA booth and discover a large portfolio of proven **PCIe IP solutions** from Gen 1 to Gen 4 for ASIC and FPGA designs.

Demonstration:

- **Switch design** comprised of 1 upstream port and 2 downstream ports that supports peer-to-peer traffic and cut-through mode.





Booth #2

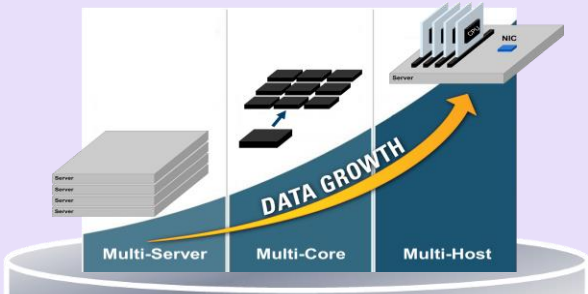
Mellanox

Exponential Data Growth – The Best Platforms Are Needed

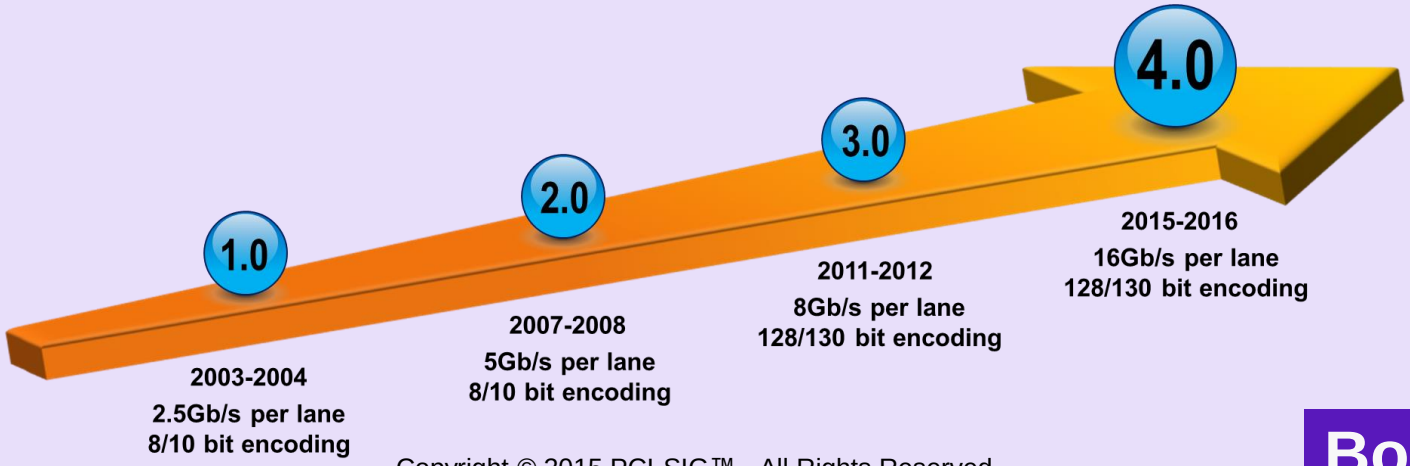
Data Needs to be Accessible Always and in Real-Time

More Devices

More Applications



More Data

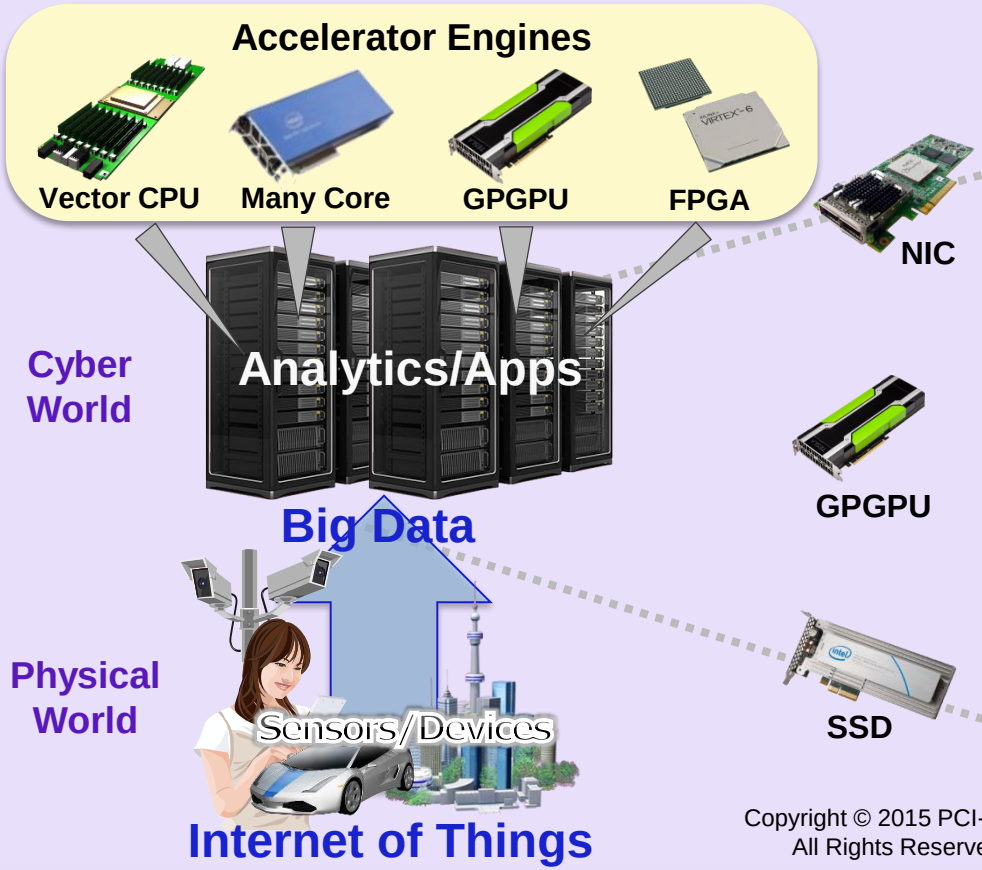


Booth #13

IO Disaggregated System with ExpEther

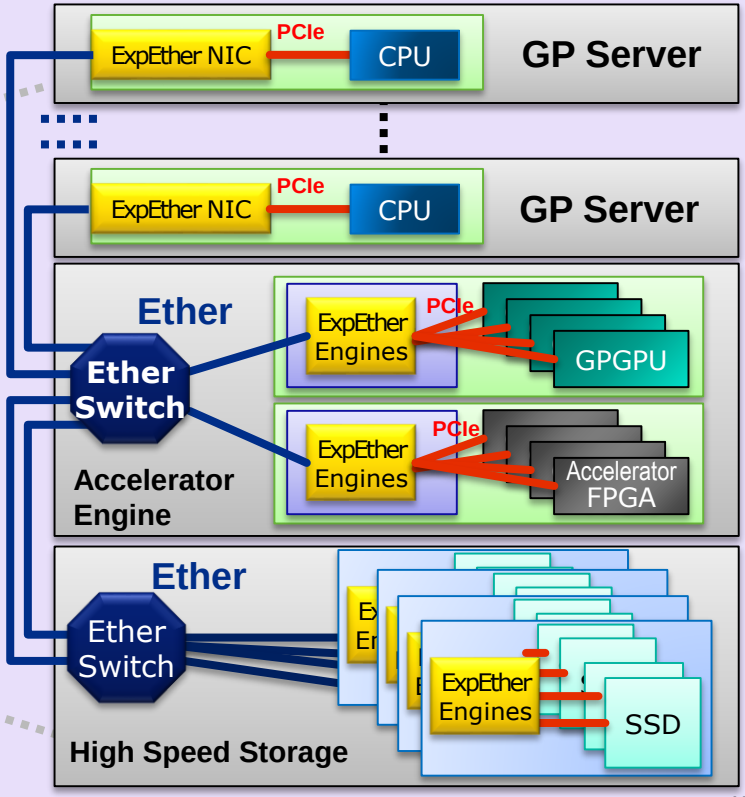
Real-Time Big Data in CPS

To accelerate data processing in the Physical World, accelerator engines are often needed in the Cyber World.



NEC Service Acceleration Platform

IO devices are disaggregated by ExpEther. NEC SA-PF can configure systems with a necessary number of GPGPUs, FPGAs and SSDs according to workload requirements



SerialTek

Demonstrations:

- Advanced PCI Express interposers for the Slot, M.2 and SFF-8639 form-factors
- NEW, unique, cost-efficient and versatile PCI Express adapters for the Slot, M.2 and SFF-8639 form-factors
- BusXpert PRO PCIe Protocol Analyzer
- BusXpert Micro PCIe Protocol Analyzer
  - Compact and Portable at 4.5 lbs; 7 x 10 x 2 inches

Applications:

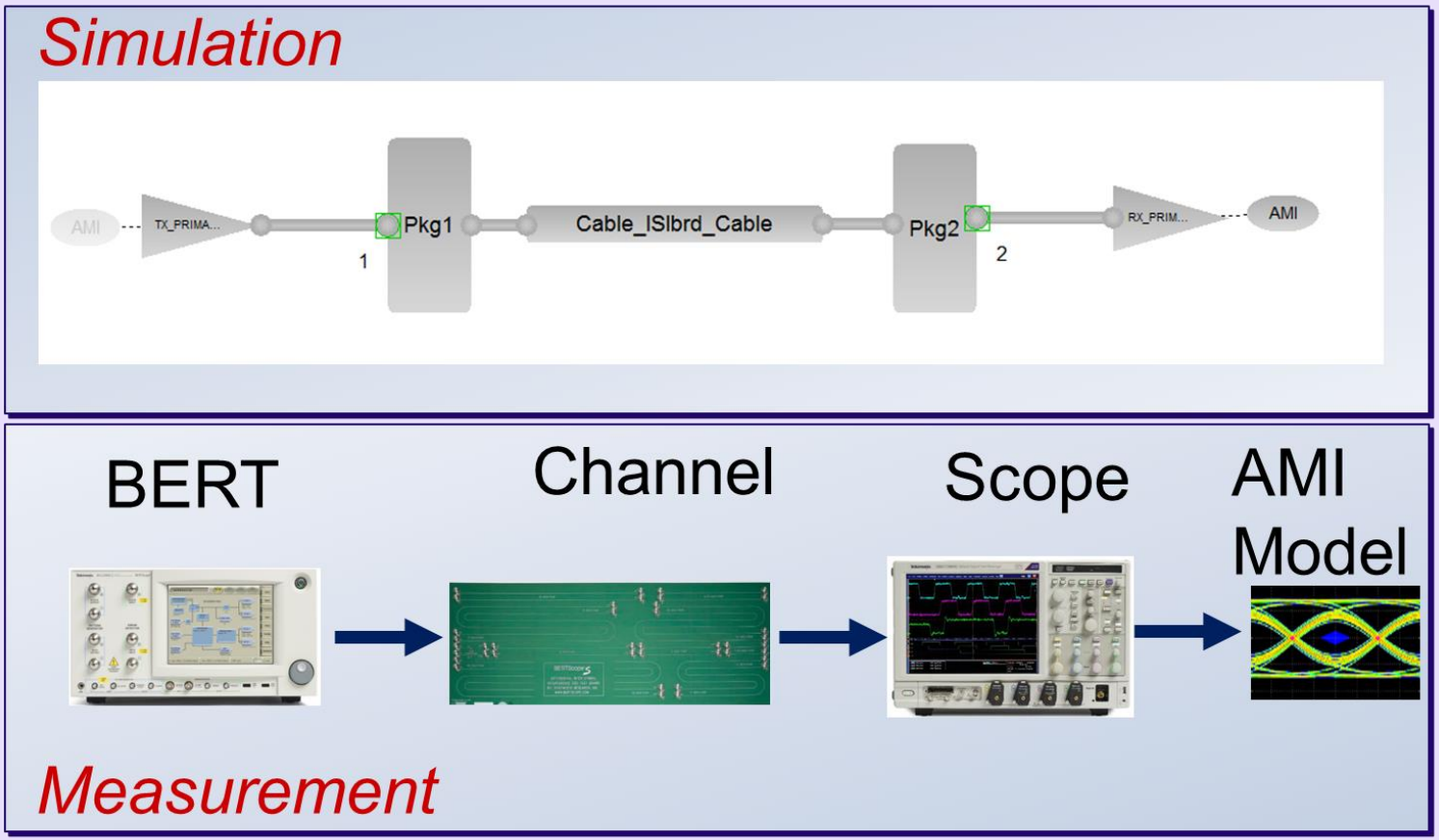
- PCIe sideband signals side-by-side with protocol decodes on the same GUI
- Oscilloscope outputs on Slot interposers

Booth #1

Tektronix

Tektronix Continues to Advance PCIe Measurements

Bridging the Simulation and Measurement Gap



Booth #11

PCI-SIG Members Exhibiting at DevCon

Platinum Sponsors

cadence™

KEYSIGHT TECHNOLOGIES

SYNOPSYS®
Silicon to Software™

TELEDYNE LECROY
Everywhereyoulook™

Gold Sponsors

avery design systems

Mentor Graphics®

samtec

Exhibitors

JDSU

Mellanox® TECHNOLOGIES

NEC

PLDA

SerialTek

Tektronix®

PCI-SIG DevCon Schedule – June 23

Lunch and Exhibit

11:30 a.m. – 1:00 p.m.

Conference Sessions

1:00 p.m. – 3:00 p.m.

Afternoon Break and Exhibit

3:00 p.m. – 3:30 p.m.

Conference Sessions

3:30 p.m. – 4:30 p.m.

Evening Mixer

5:30 p.m. – 7:00 p.m.

Conference Sessions

The following sessions are open for press attendance:

June 23	**Track 1:** PCI Express	**Track 2:** PCI-SIG Architecture	**Track 3:** Members Implementation	**Track 4:** Members Implementation
1:00 - 2:00 p.m.	PCIe 3.0 Compliance	PCIe Electrical Basics	Accurate Modelling of PCIe 3.0 Analog Buffers	PCI Express 16GT/s Design for Reliability
2:00 - 3:00 p.m.		New PCI-SIG Website	Comparing Methods for PCIe 4.0 Rx Test Calibration at 16GT/s	Testing PCIe Endpoints in Agnostic Environments
3:30 - 4:30 p.m.		PCIe Cable Update	Designing a Custom PCIe Switch	Long Tail Equalization for Future PCIe Data Rates

Questions?

Check out our revamped website!
www.pcisig.com

Back-up

PCI/PCIe Adoption in IoT

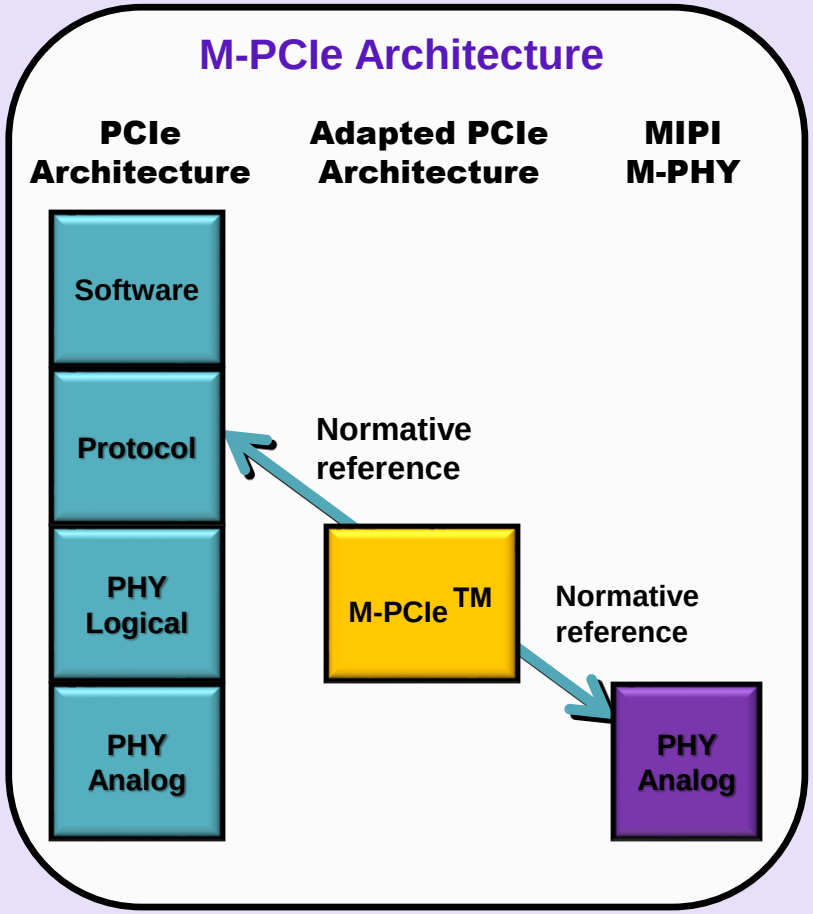
- Architecture is well-suited for low power implementations
  - ✓ Half-swing and quarter-swing
  - ✓ L1 Sub-states
  - ✓ M-PCIe™

- Protocol extension addresses SoC integration needs
  - ✓ Enhanced Allocation ECN released for member review
    - Defines mutually exclusive “Fixed BAR” capability for pre-assigned, non-re-locatable MMIO resources
  - ✓ Other ECRs are underway
- Well-understood architectural hooks in place
  - ✓ Broadly supported device discovery and enumeration
  - ✓ Extensive power management
  - ✓ Robust error model

M-PCIe for Mobile Applications

- **PCIe architecture adapted to operate over the MIPI® Alliance M-PHY® technology**

  - ✓ Extends the benefits of PCIe architecture to the mobile and handheld industry
  - ✓ Specification delivered with support for M-PHY G1/2/3
    - Seamlessly extends to Gear 4 (11.6Gbps/lane)
  - ✓ Compliance and interop scope is being investigated



M.2 for Mobile Applications

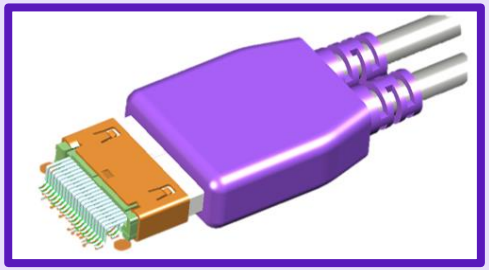
- **New generation of ultra-thin connectors for tablets and other mobile platforms**
  - ✓ Scalable performance for power-constrained platforms
  - ✓ Flexible I/O technology for balanced power and performance
  - ✓ Multiple socket definitions to support WWAN, SSD and other applications
  - ✓ Connector or soldered-down
    - – Connector: single-sided modules for low profile solutions or dual-sided modules for increased integration
    - – Soldered-down: single-sided for use in low profile applications

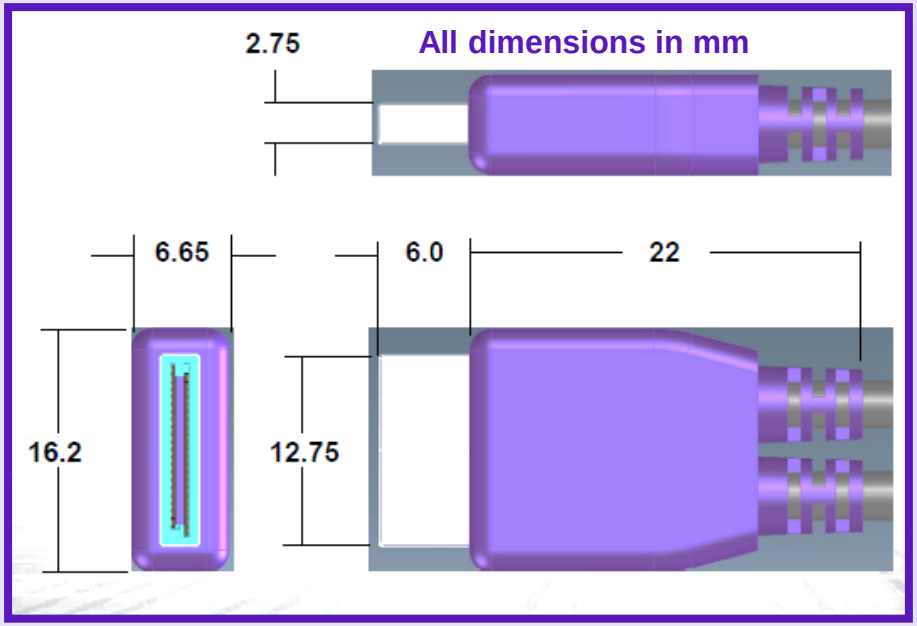
Board Width Options:
- **12mm**
- **16.5mm**
- **22mm**
- **30mm**

Board Length Options:
- **16mm**
- **26mm**
- **30mm**
- **42mm**
- **60mm**
- **80mm**
- **110mm**

OCuLink: PCIe "Outside-the-Box"

- **Low-cost, small cable form factor**
  - ✓ Optimized for internal and external enclosure usage
  - ✓ Bit rate starting at 8G with headroom to scale higher
  - ✓ Developing copper and optical cables
  - ✓ Independent reference clock with SSC technology
  - ✓ One external and one internal connector support up to four PCIe lanes
    - All cables support 8GT/s, providing up to 32 Gbps in each direction within a four lane configuration
  - ✓ Rev 0.9 currently undergoing member review
    - Final spec anticipated for Q3

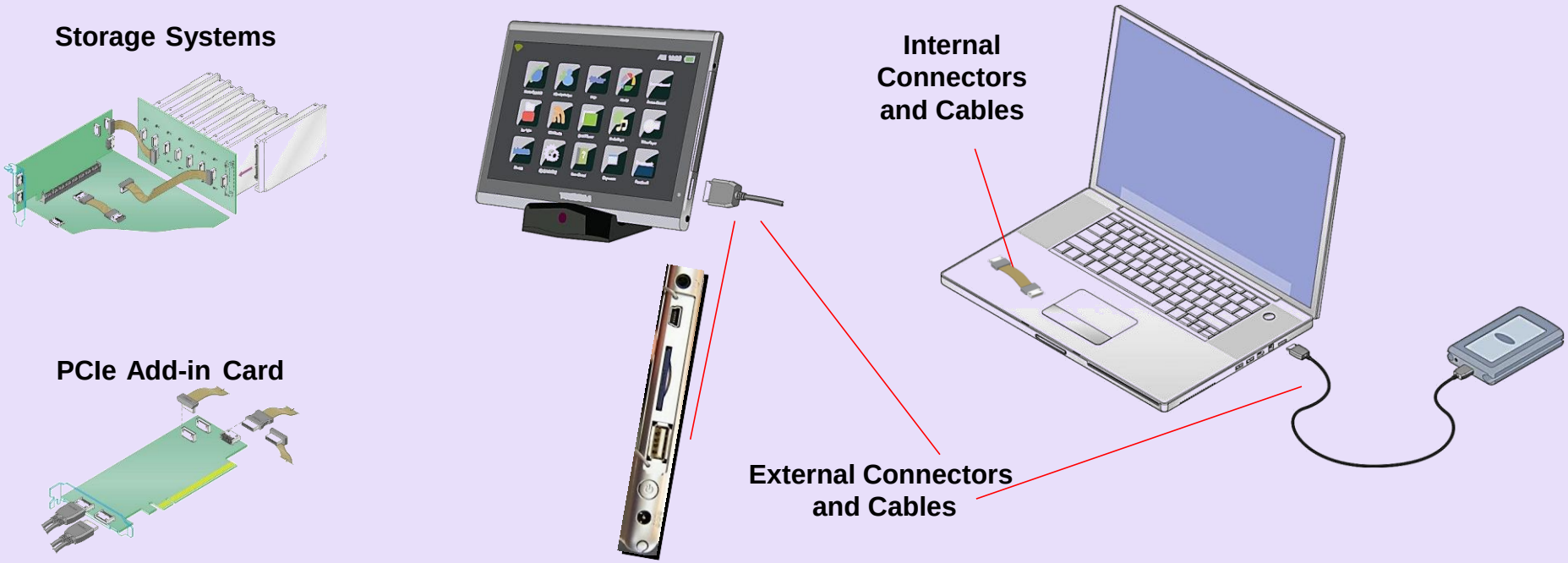




OCuLink: Usage Models

Internal usage
PCIe-attached storage

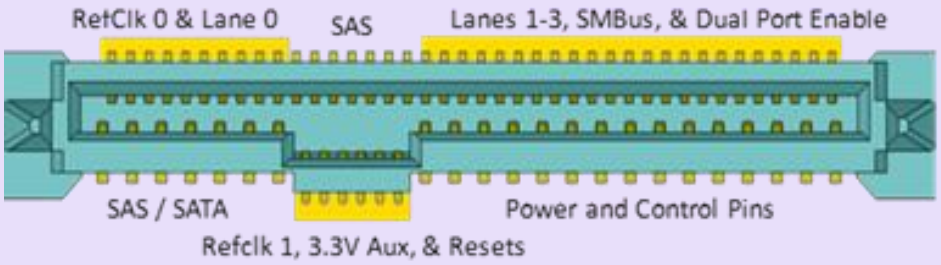
External usage
PCIe I/O expansion
External PCIe-attached storage



SFF-8639 for Storage Applications

- **Server module for high-density SSD storage attach**

  - ✓ Supports up to 8.0 GT/s data rate (per direction)
  - ✓ Enables hot plug and hot swap
  - ✓ Leverages storage industry commonality
  - ✓ Allows co-existence of both SFF-8639 devices and existing storage products
  - ✓ Extensible for future bandwidth needs
  - ✓ Maximizes SFF-8639 module interoperability for user flexibility
  - ✓ Revision 0.9 undergoing review



SFF-8639 Dimensions

- Length: 100.45mm
- Width: 69.85mm
- Height: 7mm